ABSTRACT

A clock compensation circuit is provided. The circuit comprises a clock synchronization circuit coupled to receive an input clock signal, wherein the clock synchronization circuit generates a master clock signal and produces a plurality of internal logic clock signals. The circuit further comprises a phase comparator coupled to receive one of the plurality of internal logic clock signals and a sample clock from an associated receiver, wherein the phase comparator generates a control signal based on a phase comparison between the sample clock and the one of the plurality of internal logic clock signals and a down converter channel coupled to receive each of the plurality of internal logic clock signals and the control signal and to pass data in phase with the sample clock using the internal logic clock signal based on the control signal.